CA-IS309X 5-kV$_{RMS}$ Isolated Half-Duplex RS-485 Transceivers With Isolated DC-DC Power Supply

1. Features

- Meets TIA/EIA-485-A Requirements
- Integrated DC-DC Power Supply
  - 3.3V/5V Output
  - $V_{ISO} \leqslant V_{CC}$
  - Soft-start to Suppress Inrush Current
  - Over-Current and Short Circuit Protection
  - Over Temperature Protection
- Robust Electro-Magnetic Compatibility (EMC)
- Up to 10 Mbps
- Fail-safe Receiver for Bus Open, Short
- Up to 256 Nodes on a Bus
- Bus-Pin ESD Protection:
  - 8kV HBM
  - ±15 kV IEC 61000-4-2 Contact Discharge
- 3V to 5.5V Input Voltage (V_{CC})
- RO Logic High When Bus Side Open or Short Circuit in Receiver Mode
- Wide Operating Temperature Range: -40°C to 125°C
- Pinouts Compatible with Most RS-485 and RS-422 Transceivers
- High CMTI: ±150 kV/μs (Typical)
- Isolation Rating up to 5.0 kV$_{RMS}$ Isolation Barrier Life: > 40 Years
- RoHS-Compliant SOIC16-WB(W) and SOIC20-WB(T) Wide Body Package
- Safety-Related Certifications (Pending):
  - DIN V VDE V 0884-11: 2017-01 V_{IOTM} = 7071 V_{PK} and V_{IORM} = 849 V_{PK}
  - 5000 VRMS for 1 Minute per UL 1577
  - IEC 60950, IEC 60601 and EN 61010 Certifications
  - CQC, TUV and CSA Certifications

2. Applications

- Isolated RS-485 and RS-422 Interfaces
- Solar Inverter
- Motor Driver Control

3. General Description

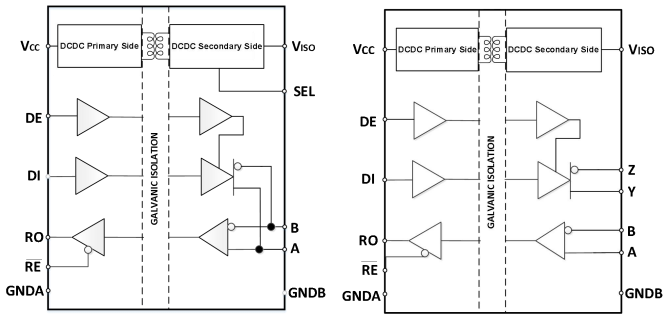
CA-IS3092 and CA-IS3098 devices are isolated half-duplex RS-485 and RS-422 transceivers with high reliability, low EMI and strong anti-interference capability from magnetic changes. The receiver input has fail-safe features ensuring that the output is low when the input is open or shorted. CA-IS3090 and CA-IS3096 devices are isolated full-duplex RS-485 and RS-422 transceivers

The CA-IS309x devices have high insulation capability to handle noise and surge on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry. High CMTI ability promises the correct transmission of signal. CA-IS309xW are available in a 16-lead wide-body SOIC package. CA-IS309xT are available in a 20-lead wide-body SOIC package. CA-IS309x provide up to 5 kV$_{RMS}$ of isolation.

Table 3- 1 Device Information

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CA-IS3090W CA-IS3092W CA-IS3096W CA-IS3098W	SOIC16-WB(W)	10.30 mm × 7.50 mm
CA-IS3090T CA-IS3096T	SOIC20-WB(W)	12.80 mm X 7.50 mm

Figure 3- 1 CA-IS309x Function Diagram



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4. Ordering Guide

Table 4- 1 Ordering Guide for Valid Ordering Part Number

Ordering Part Number	Mode	Data Rate (Mbps)	V_{ISO} (V)	Package
CA-IS3090W	Full-Duplex	0.5	3.3	SOIC16-WB(W)
CA-IS3092W	Half-Duplex	0.5	3.3/5.0	SOIC16-WB(W)
CA-IS3096W	Full-Duplex	10	3.3	SOIC16-WB(W)
CA-IS3098W	Half-Duplex	10	3.3/5.0	SOIC16-WB(W)
CA-IS3090T	Full-Duplex	0.5	3.3	SOIC20-WB(W)
CA-IS3096T	Full-Duplex	10	3.3	SOIC20-WB(W)

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5. History

Preliminary Version

6. Pin Description and Functions

6.1. CA-IS3090W/CA-IS3096W Description

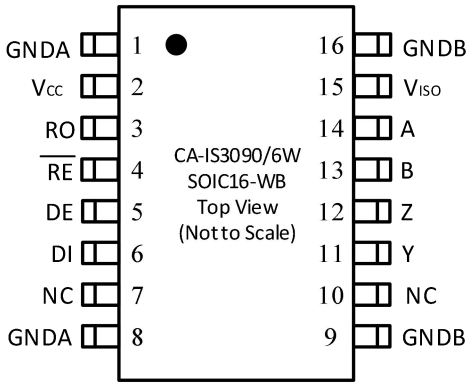


Figure 6- 1 CA-IS3090W/CA-IS3096W Top View

Table 6- 1 CA-IS3090W/CA-IS3096W Pin Description and Functions

Name	PIN Number	Type	Description
GNDA	1	GND	Ground of logic side
VCC	2	Supply	Power supply of logic side
RO	3	Logic Output	Receiver output
$\overline{RE}$	4	Logic Input	Receiver enable input
DE	5	Logic Input	Driver enable input, high effective while keeps driver output in a high impedance state when it is low
DI	6	Logic Input	Driver input
NC	7	-	No connect
GNDA	8	GND	Ground of logic side
GNDB	9	GND	Ground of bus side
NC	10	-	No connect
Y	11	Bus I/O	Transmitter non-inverting output
Z	12	Bus I/O	Transmitter inverting output
B	13	Bus I/O	Receiver inverting input
A	14	Bus I/O	Receiver non-inverting input
V_{ISO}[1]	15	Supply	Output of isolated DC-DC power supply
GNDB	16	GND	Ground of bus side

1. V_{ISO}[1] =3.3V

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6.2. CA-IS3092W/ CA-IS3098W Description

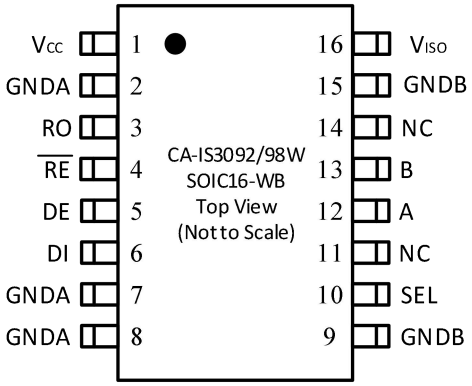


Figure 6- 2 CA-IS3092W/CA-IS3098W SOIC16 Top View

Table 6- 2 CA-IS3092W/CA-IS3098W Pin Description and Functions

Name	PIN Number	Type	Description
V_{CC}	1	Supply	Power supply of logic side
GNDA	2	GND	Ground of logic side
RO	3	Logic Output	Receiver output
$\overline{RE}$	4	Logic Input	Receiver enable input
DE	5	Logic Input	Driver enable input, high effective while keeps driver output in a high impedance state when it is low
DI	6	Logic Input	Driver input
GNDA	7	GND	Ground of logic side
GNDA	8	GND	Ground of logic side
GNDB	9	GND	Ground of bus side
SEL[1]	10	Logic Input	V_{ISO} output voltage select Pin
NC	11	-	No connect
A	12	Bus I/O	Transmitter non-inverting input
B	13	Bus I/O	Transmitter inverting input
NC	14	-	No connect
GNDB	15	GND	Ground of bus side
V_{ISO}	16	Supply	Output of isolated DC-DC power supply

1. When SEL is connected to V_{ISO} Pin, V_{ISO}=5.0V. When SEL is connected to GNDB or floating, V_{ISO}=3.3V. When V_{CC}=3.3V, SEL Pin must be floating or connected to GNDB. When V_{CC}=5.0V, there is no connection limit on SEL Pin.

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6.3. CA-IS3090T/CA-IS3096T Description

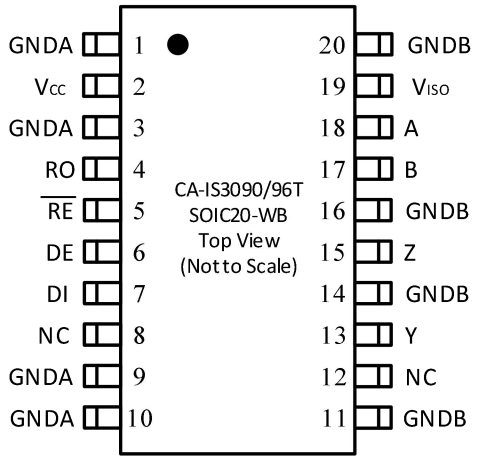


Figure 6- 3 CA-IS3090T/CA-IS3096T SOIC20 Top View

Table 6- 3 CA-IS3090T/CA-IS3096T Pin Description and Functions

Name	PIN Number	Type	Description
GNDA	1	GND	Ground of logic side
V_{CC}	2	Supply	Power supply of logic side
GNDA	3	GND	Ground of logic side
RO	4	Logic Output	Receiver output
$\overline{RE}$	5	Logic Input	Receiver enable input
DE	6	Logic Input	Driver enable input, high effective while keeps driver output in a high impedance state when it is low
DI	7	Logic Input	Driver input
NC	8	-	No connect
GNDA	9	GND	Ground of logic side
GNDA	10	GND	Ground of logic side
GNDB	11	GND	Ground of bus side
NC	12	-	No connect
Y	13	Bus I/O	Transceiver noninverting output
GNDB	14	GND	Ground of bus side
Z	15	Bus I/O	Transceiver inverting output
GNDB	16	GND	Ground of bus side
B	17	Bus I/O	Receiver inverting input
A	18	Bus I/O	Receiver noninverting input
V_{ISO}[1]	19	Supply	Output of isolated DC-DC power supply
GNDB	20	GND	Ground of bus side

1. V_{ISO}[1] =3.3V

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7. Specifications

7.1. Absolute Maximum Ratings[1]

PARAMETER		MIN	MAX	UNIT
V_{CC}, V_{ISO}	Supply Voltage[2]	-0.5	6.0	V
V_{in}	Voltage input at any DE, DI or $\overline{RE}$ pin	-0.5	V_{CC}+0.5[3]	V
I_O	Output current	-20	20	mA
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-65	150	°C

NOTE:

1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
3. Maximum voltage must not exceed 6 V.

7.2. ESD Ratings

PARAMETER			VALUE	UNIT
V_{ESD} Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[1]	Bus pins and GNDA	±6000	V
		Bus pins and GNDB	±8000	
		All pins	±6000	
	Contact discharge, per IEC 61000-4-2, Bus pins and GNDB		±15000	
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[2]		±2000	

NOTE:

1. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
2. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3. Recommended Operating Conditions

PARAMETER		Min	Typ	Max	Unit
V_{CC}[1]	Supply voltage of logic side	3	3.3	5.5	V
V_{OC}	Voltage at either bus I/O pin	-7		12	V
V_{ID}	Differential input voltage (A with respective to B)	-12		12	V
V_{IH}	High-level input voltage (DE, DI or $\overline{RE}$)	2.0			V
V_{IL}	Low-level input voltage (DE, DI or $\overline{RE}$)			0.8	V
DR	CA-IS3090W Data Rate			0.5	Mbps
DR	CA-IS3092W Data Rate			0.5	Mbps
DR	CA-IS3096W Data Rate			10	Mbps
DR	CA-IS3098W Data Rate			10	Mbps
DR	CA-IS3090T Data Rate			0.5	Mbps
DR	CA-IS3096T Data Rate			10	Mbps
T_A	Ambient Temperature	-40	25	125	°C

NOTE:

1. V_{CC} should be higher than V_{ISO}。

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7.4. Thermal Information

THERMAL METRIC		CA-IS309x		Unit
		T	W	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	83.4	86.5	°C/W

7.5. Insulation Specifications

PARAMETER		TEST CONDITIONS	VALUE W/T	UNIT
CLR	External clearance[1]	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage[1]	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	21	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>400	V
	Material group	According to IEC 60664-1	II	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V_{RMS}	I-IV	
		Rated mains voltage ≤ 400 V_{RMS}	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-III	
DIN V VDE V 0884-11:2017-01[2]				
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	849	V_{PK}
V_{IOWM}	Maximum isolation working voltage	AC voltage (sine wave);Time dependent dielectric breakdown(TDDB) Test	600	V_{RMS}
		DC Voltage	849	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{IOTM}$, t= 1 s (100% production)	7070	V_{PK}
V_{IOSM}	Maximum surge isolation voltage[3]	Test method per IEC 60065, 1.2/50 µs waveform, VTEST = 1.6 × VIOSM (qualification)	6250	V_{PK}
q_{pd}	Apparent charge[4]	Method a，After I/O safety test subgroup, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	pC
		Method a，after environmental tests subgroup1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤5	
		Method b1, At routine test (100% production) and preconditioning (Type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤5	
C_{IO}	Barrier capacitance, input to output[5]	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~0.5	pF
R_{IO}	Pollution degree	V_{IO} = 500 V, T_A = 25°C	$>10^{12}$	Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ 125°C	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150°C	$>10^{9}$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	5000	V_{RMS}

NOTE:

1. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.
2. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
3. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
4. Apparent charge is electrical discharge caused by a partial discharge (pd).
5. All pins on each side of the barrier tied together creating a two-terminal device.

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7.6. Safety-Related Certifications

VDE (Pending)	CSA (Pending)	UL (Pending)	CQC (Pending)	TUV (Pending)
Certified according to DIN V VDE V 0884-11:2017-01	Certified according to IEC 60950-1, IEC 62368-1 and IEC 60601-1	Recognized under UL 1577 Component Recognition Program	Certified according to GB4943.1-2011	Certified according to EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2:2013

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7.7. Electrical Characteristics

7.7.1. Driver

All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = -40°C to 125°C, V_{CC} = 5 V unless otherwise noted.

Parameter		Test Condition	Min	Typ	Max	Unit
$\|V_{OD1}\|$	Differential output voltage	I_O=0mA, No load	3.09	3.35	3.62	V
$\|V_{OD2}\|$	Differential output voltage	R_L=54Ω, Figure 10- 1	1.17	1.4		V
		R_L=100Ω, Figure 10- 1	1.7	2		
$\|V_{OD3}\|$	Differential output voltage	V_{test} from -7Vto 12V， Figure 10- 3	1	1.4		V
$\Delta\|V_{OD}\|$	Change of the differential output voltage	R_L=54Ω, or R_L=100Ω, Figure 10- 1	-0.2		0.2	V
V_{OC}	Steady-state common-mode output voltage	R_L=54Ω, or R_L=100Ω, Figure 10- 1	1		3	V
ΔV_{OC}	Change in steady-state common-mode output voltage	R_L=54Ω, or R_L=100Ω, Figure 10- 1			0.2	V
V_{IH}	Input threshold when logic is high	DI,DE, $\overline{RE}$	2.0			V
V_{IL}	Input threshold when logic is Low	DI,DE, $\overline{RE}$			0.8	V
I_{IL}	Input leakage current	DI,DE, $\overline{RE}$=0 OR 1	-20		20	μA
I_{OZ}	Output leakage current in high impedance (Y,Z)	DE=0, $\overline{RE}$=0,V_{CC}=0 或 5V,V_{IN}=12V		60	100	μA
		DE=0, $\overline{RE}$=0,V_{CC}=0 或 5V,V_{IN}=-7V	-100	-60		
I_{os1}	Short-circuit output current (V_O = HIGH)	DE= $\overline{RE}$=1, DI=1, V_Y=-7 V, V_Z=12 V	29	44	62	mA
I_{os2}	Short-circuit output current (V_O = LOW)	DE= $\overline{RE}$ =1, DI=0, V_Y=-7 V, V_Z=12 V	29	44	62	mA
CMTI	Common-mode transient immunity	V_{CM} = 1200V, Figure 10- 9	100	150		kV/μS
C_I	Input capacitance	VI = VCC/ 2 + 0.4×sin(2πft), f = 1 MHz, VCC = 5 V		2		pF

7.7.1. Receiver

All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = -40°C to 125°C, V_{CC} = 5 V unless otherwise noted.

Parameter		Test Condition	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	V_{CC}=5V， I_{OH}=4mA	V_{CC}-0.4	4.8		V
V_{OH}	High-level output voltage	V_{CC}=3.3V， I_{OH}=-4mA	V_{CC}-0.4	3		V
V_{OL}	Low-level output voltage	V_{CC}=5V， I_{OL}=4mA		0.2	0.4	V
V_{OL}	Low-level output voltage	V_{CC}=3.3V， I_{OL}=4mA		0.2	0.4	V
$V_{IT+(IN)}$	Positive-going input threshold voltage			-100	-20	mV
$V_{IT-(IN)}$	Negative-going input threshold voltage		-200	-130		mV
$V_{I(HYS)}$	Hysteresis voltage			30		mV
I_I	Bus input current	V_A or V_B =12V, Other input = 0 V		0.04	0.1	mA
		V_A or V_B =12V, VCC = 0 V, other input = 0 V		0.06	0.13	
		V_A or V_B = –7 V, Other input = 0 V	-0.1	-0.04		
		V_A or V_B = –7 V, VCC = 0 V, other input = 0 V	-0.1	-0.03		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V			20	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V	-20			μA
R_{ID}	Differential input resistance	A,B, -7V<V_{CM}<12V	384	430	478	KΩ

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C_D	Differential input capacitance	Test input signal is a 1.5-MHz sine wave with 1-V_{PP} amplitude and C_D is measured across A and B		7		pF
C_I	Input capacitance to ground	V_{IO} = 0.4 × sin (2πft), f = 1 MHz		2		pF

7.8. Supply Current

All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = -40°C to 125°C, V_{CC} = 5 V unless otherwise noted.

Parameter		Test Condition	Min	Typ	Max	Unit
V_{ISO}	Isolated DC-DC output voltage	V_{CC}=5V, No load across Y and Z,	3.17	3.35	3.53	V
I_{CC}	Supply current in logic side	V_{CC}=3.3V,No load across Y and Z, /RE=0 ,DE=1 ,DI=0	10	15	19	mA
		V_{CC}=5.0V, No load across Y and Z, /RE=0 ,DE=1 ,DI=0	9	13	17	mA
		V_{CC}=3.3V, R_L=100Ω, /RE=0 ,DE=1 ,DI=0	50	55	60	mA
		V_{CC}=5V, R_L=100Ω, /RE=0 ,DE=1 ,DI=0	43	48	53	mA
		V_{CC}=3.3V, R_L=54Ω, /RE=0 ,DE=1 ,DI=0	62	69	76	mA
		V_{CC}=5V, R_L=54Ω, /RE=0 ,DE=1 ,DI=0	45	49	53	mA
		V_{CC}=3.3V, R_L=120Ω, /RE=0 ,DE=1 ,DI=0	45	50	55	mA
		V_{CC}=5V, R_L=120Ω, /RE=0 ,DE=1 ,DI=0	32	36	40	mA
		R_L=54Ω, V_{CC}=3.3V,/RE=0,DE=1,DI apply 5MHz with 50% Duty square-wave	69	73	77	mA
		R_L=54Ω, V_{CC}=5.0V,/RE=0,DE=1, DI apply 5MHz with 50% Duty square-wave	42	50	53	mA
		R_L=100Ω, V_{CC}=3.3V,/RE=0,DE=1, DI apply 5MHz with 50% Duty square-wave	58	61	64	mA
		R_L=100Ω, V_{CC}=5.0V,/RE=0,DE=1, DI apply 5MHz with 50% Duty square-wave	40	43	46	mA
		R_L=120Ω, V_{CC}=3.3V,/RE=0,DE=1,DI DI apply 5MHz with 50% Duty square-wave	53	58	63	mA
		R_L=120Ω, V_{CC}=5.0V,/RE=0,DE=1,DI DI apply 5MHz with 50% Duty square-wave	38	42	46	mA

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7.9. Switching Characteristics

7.9.1. Driver

All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = -40°C to 125°C, V_{CC} = 5 V unless otherwise noted.

参数		测试说明	最小值	典型值	最大值	单位
t_{PLH}, t_{PHL}	Propagation delay	Figure 10- 3, Figure 10- 4, Figure 10- 8, R_{diff}=54Ω, C_{L1}=C_{L2}=50pF		16	48	ns
PWD	Pulse width distortion, $\|t_{PLH} - t_{PHL}\|$			3	12.5	ns
t_r	Rising time of differential output signal			12	25	ns
t_f	Falling time of differential output signal			12	25	ns
t_{PZH}/ t_{PZL}	Propagation delay for driver enable			28	90	ns
t_{PHZ}/ t_{PLZ}	Propagation delay for driver disable			28	90	ns

7.9.1. Receiver

All minimum/maximum specifications apply over the entire recommended operation range, unless otherwise noted. All typical specifications are at T_A = -40°C to 125°C, V_{CC} = 5 V unless otherwise noted.

参数		测试说明	最小值	典型值	最大值	单位
t_{PLH}, t_{PHL}	Propagation delay	Figure 10- 5, Figure 10- 6, Figure 10- 7, R_{diff}=54Ω, C_{L1}=C_{L2}=50pF		80	165	ns
PWD	Pulse width distortion, $\|t_{PLH} - t_{PHL}\|$			15	30	ns
t_r	Rising time of differential output signal			2.5	4	ns
t_f	Falling time of differential output signal			2.5	4	ns
t_{PHZ}, t_{PLZ}	Propagation delay for receiver enable			28	90	ns
t_{PZH}, t_{PZL}	Propagation delay for receiver disable			43	52	ns

8. Input Equivalent Circuit

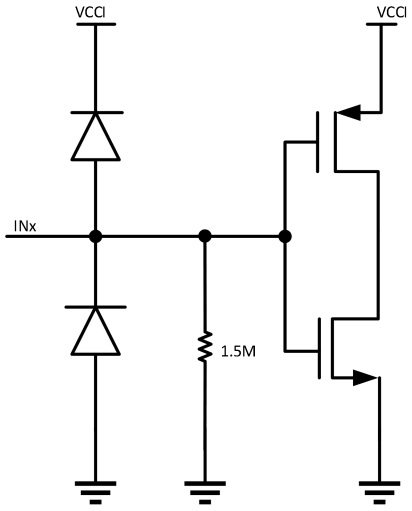


Figure 8- 1 Input Equivalent Circuit

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9. Detailed Description

9.1. Overview

The CA-IS3090/96 devices are isolated full-duplex transceivers with fail-safe, over current protection and over temperature functions, which support RS-485 and RS-422. The CA-IS3092/98 devices are isolated half-duplex transceivers with fail-safe, over current protection and over temperature functions, which support RS-485 and RS-422.

9.2. Fail-Safe Features

The CA-IS309x devices guarantee the output of receiver to go failsafe-low when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus). This is realized by setting the positive- and negative-going input threshold voltage of receiver to –100 mV and –130 mV respectively. When the differential input voltage of the receiver ($V_{ID} = V_A – V_B$) is higher than positive-going input threshold V_{IT+}, the receiver output (RO) turns high. When V_{ID} is lower than negative-going input threshold V_{IT-}, RO turns low. And this setting meets TIA/EIA-485-A standard requirement. When all the transceivers on a bus are forbidden and not active, V_{ID} is pulled to 0 V via termination resistors.

9.3. Up to 256 Nodes on a Bus

Standard-compliant RS-485 transceivers must be able to drive 32 unit loads where 1 unit load represents a load impedance of approximately 12 kΩ. The CA-IS309x devices consists of 1/8 unit load transceivers and could connect up to 256 nodes on a bus. These devices could be combined with themselves or other RS-485 transceivers on a bus arbitrarily as long as the total load exceeds no more than 32 unit loads.

9.4. Driver Output Protection

The CA-IS309x devices adopt two mechanisms to avoid excessive current or power dissipation during bus fault or conflict conditions:

1) over current protection in the full range of the common-mode voltage to provide fast short-circuit protection.

2) thermal sensing circuitry detects the die temperature and would force the driver to output low-level when a die temperature of 160 °C (typical) is reached.

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10. Parameter Measurement Information

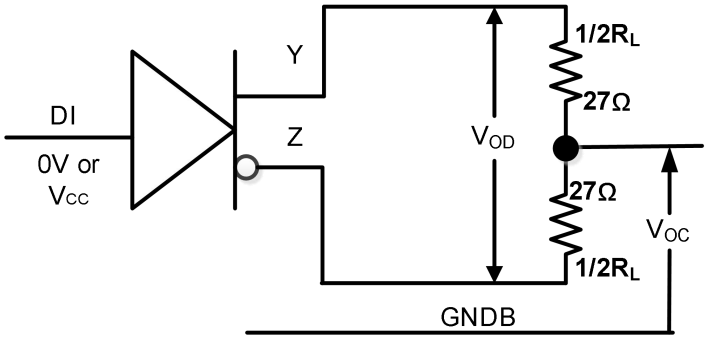


Figure 10- 1 Driver Voltage Test Circuit

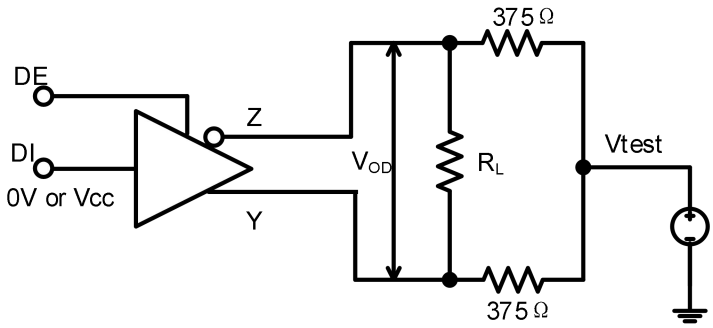
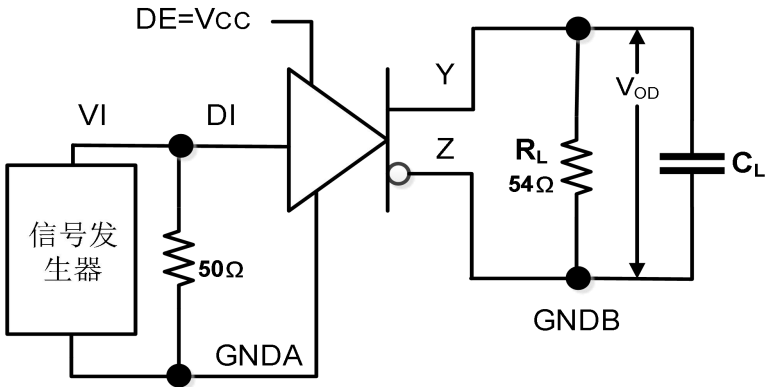


Figure 10- 2 Driver Voltage Test Circuit Under Common Mode Load



NOTE:

1. 50-Ω resistor is used for match in the test and does not need in practical implementations;
2. C_L includes fixture and instrumentation capacitance.

Figure 10- 3 Driver Switching Test Circuit

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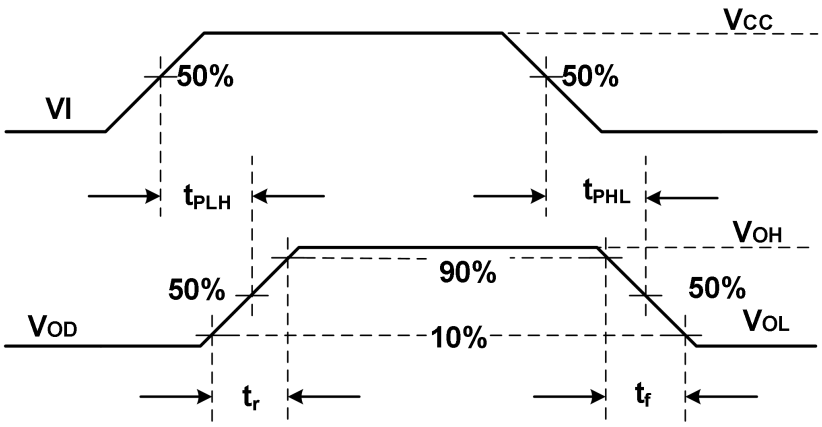
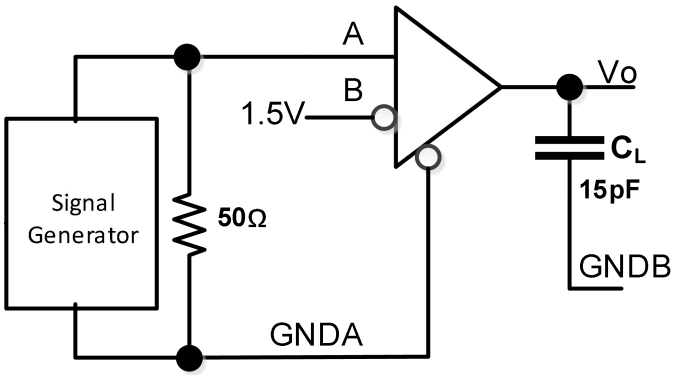


Figure 10- 4 Driver Switching Voltage Waveforms



NOTE:

1. 50-Ω resistor is used for match in the test and does not need in practical implementations;
2. C_L includes fixture and instrumentation capacitance.

Figure 10- 5 Receiver Switching Test Circuit

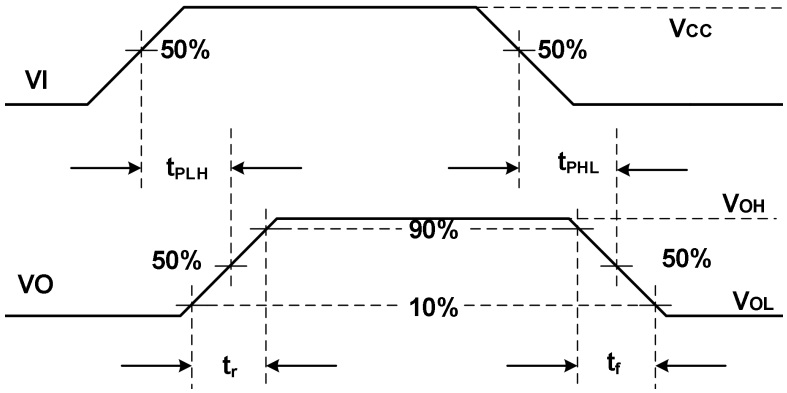


Figure 10- 6 Receiver Switching Voltage Waveforms

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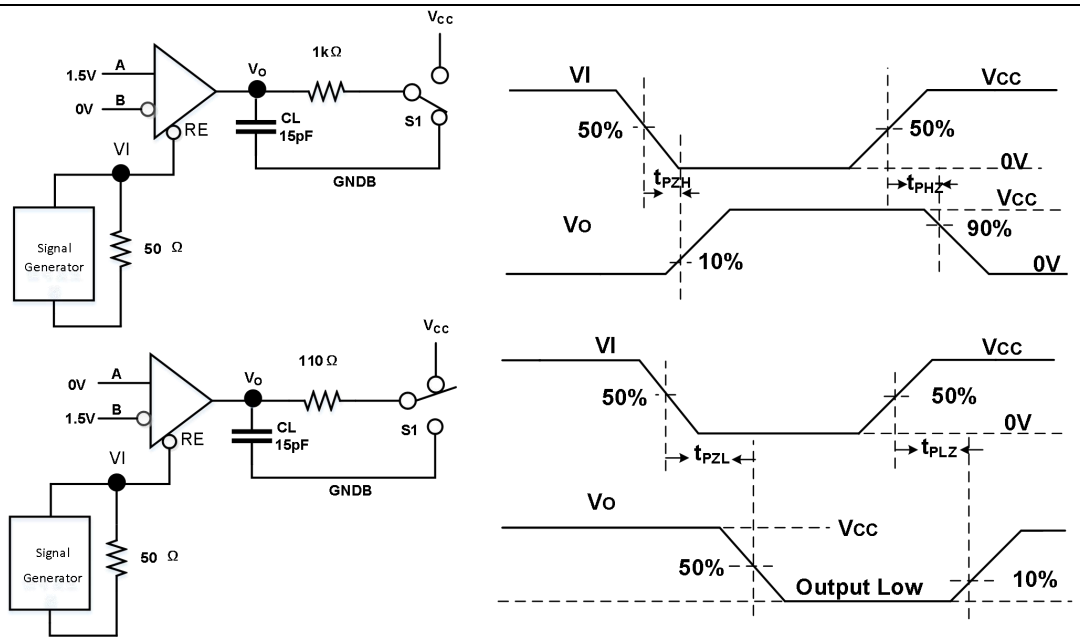


Figure 10- 7 Receiver Enable Test Circuit and Voltage Waveforms

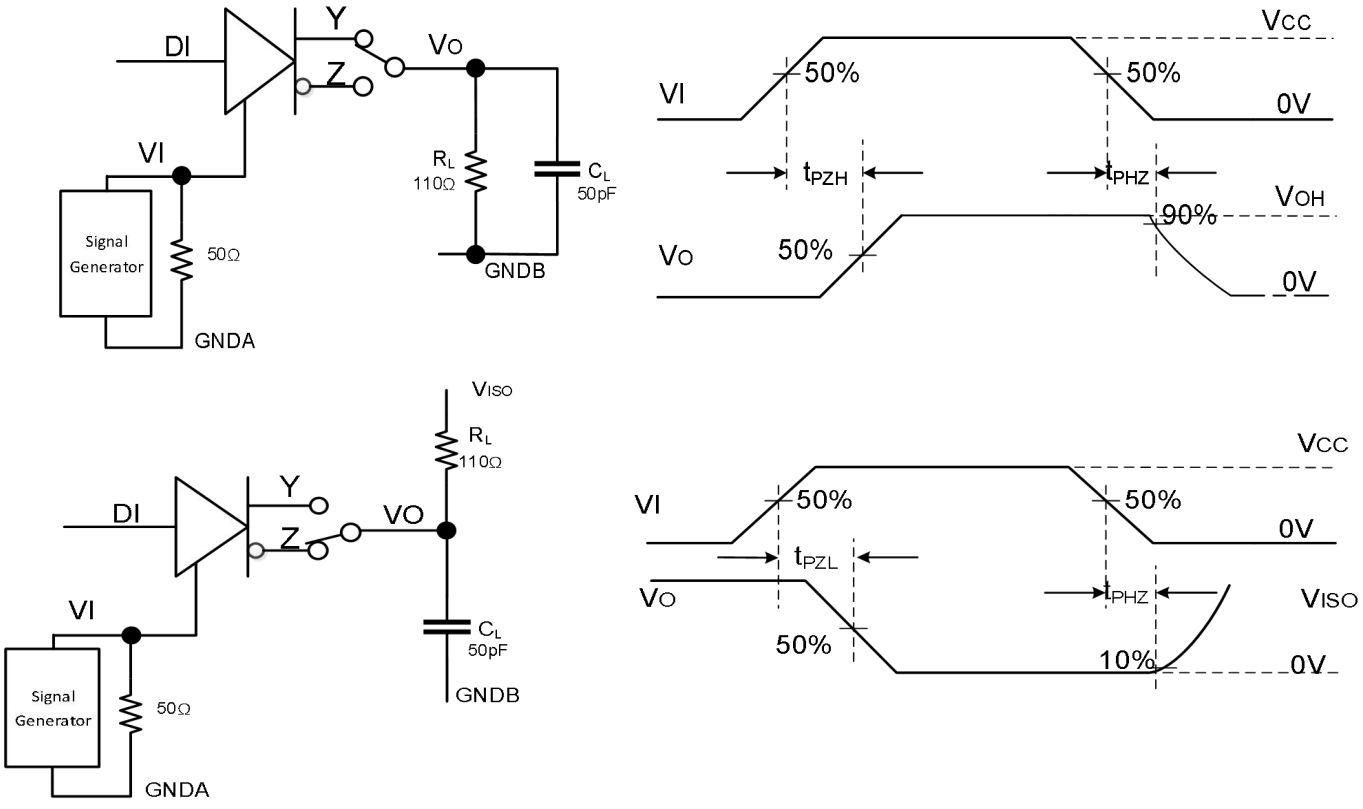


Figure 10- 8 Driver Enable and Disable Test Circuit and Voltage Waveforms

NOTE:

1. 50-Ω resistor is used for match in the test and does not need in practical implementations;
2. C_L includes fixture and instrumentation capacitance.

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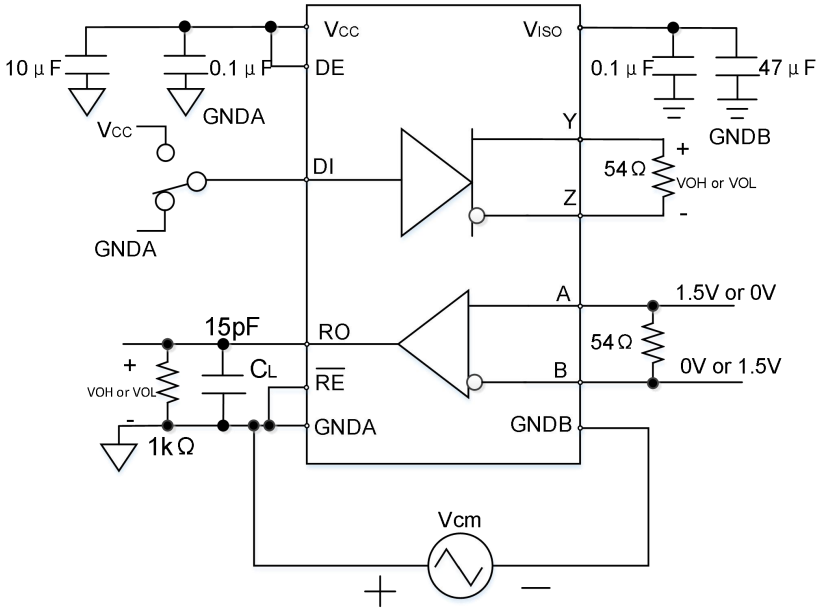


Figure 10- 9 Common-Mode Transient Immunity Test Circuit in Full Duplex mode

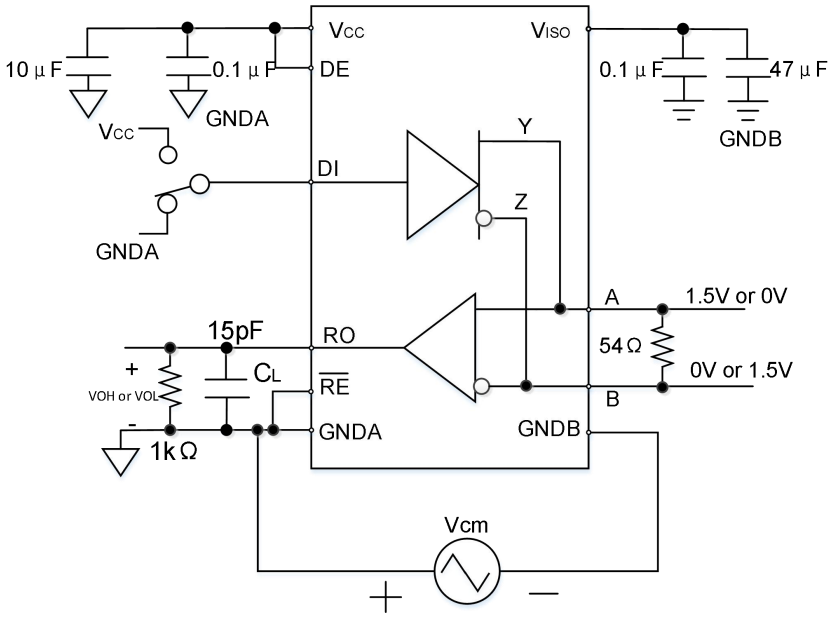


Figure 10- 10 Common-Mode Transient Immunity Test Circuit in Half Duplex mode

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11. Functional Modes

错误!未找到引用源。 lists the driver functional modes and 错误!未找到引用源。 lists the receiver functional modes of CA-IS309x.

Table 11- 1 Driver Function Truth Table

INPUT		OUTPUTS	
(DI)	(DE)	Y	Z
H	H	H	L
L	H	L	H
X	L	Hi-Z	Hi-Z
X	OPEN	Hi-Z	Hi-Z
OPEN	H	H	L
X	X	Hi-Z	Hi-Z

NOTE:

1. $\overline{RE}$ connects to logic high when the driver is enabled；
2. PU = Powered Up; PD = Powered Down; X = Irrelevant; H = Logic High; L = Logic High; Hi-Z = High Impedance.

Table 11- 2 Receiver Function Truth Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT
$V_{ID} = (V_A - V_B)$	$(\overline{RE})$	(R)
-0.02 V ≤ V_{ID}	L	H
-0.2 V < V_{ID} < -0.02 V	L	?
V_{ID} ≤ -0.2 V	L	L
X	H	Hi-Z
X	OPEN	Hi-Z
Open circuit	L	H
Short circuit	L	H
Idle(terminated)bus	L	H

NOTE:

1. DE connects to logic low when the receiver is enabled；
2. PU = Powered Up; PD = Powered Down; X = Irrelevant; H = Logic High; L = Logic High; Hi-Z = High Impedance; ? = Indeterminate

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12. Application

CA-IS309xT need 0.1μF and 10μF input cap by the input Pin Vcc and output Pin V_{ISO}. The input and output cap should be placed by the input and output Pin as close as possible.is CA-IS309xT typical application circuit and is CA-IS309xW typical application circuit.
It is strongly recommended that to choose 47μF capacitor as the output cap and there is no any input signal at the logic side when CA-IS309x is powering up.

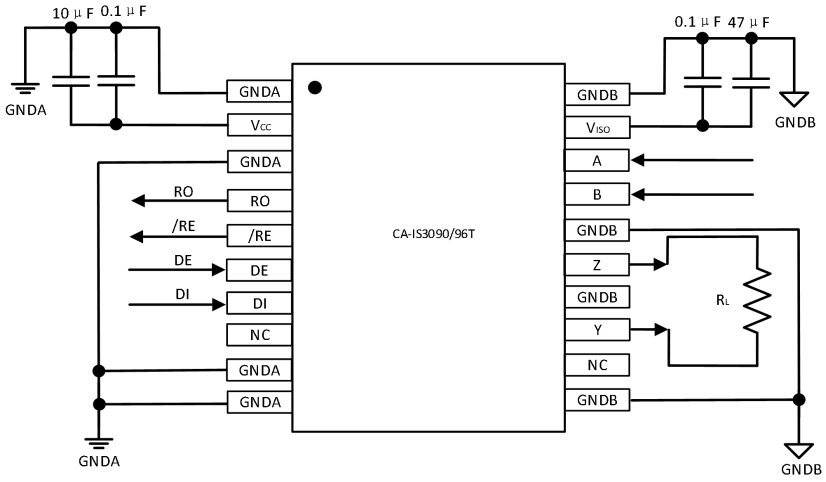


Figure 12- 1 CA-IS3090/96T Typical Application Circuit

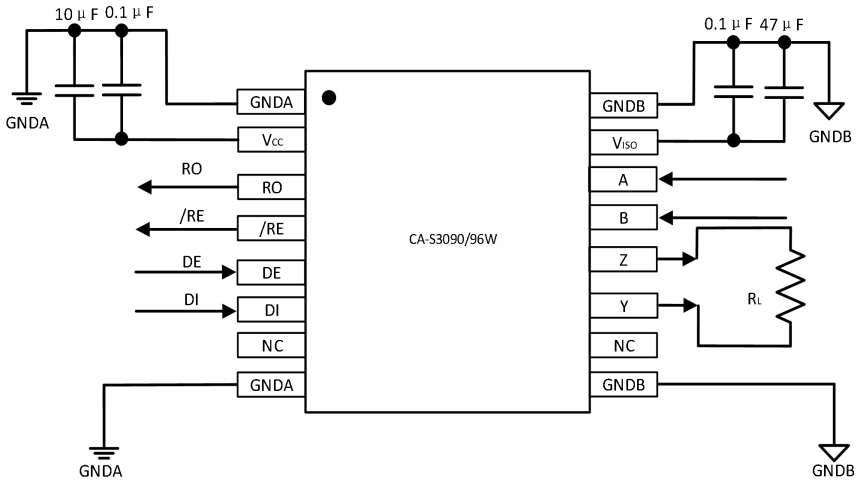


Figure 12- 2 CA-IS3090/96W Typical Application Circuit

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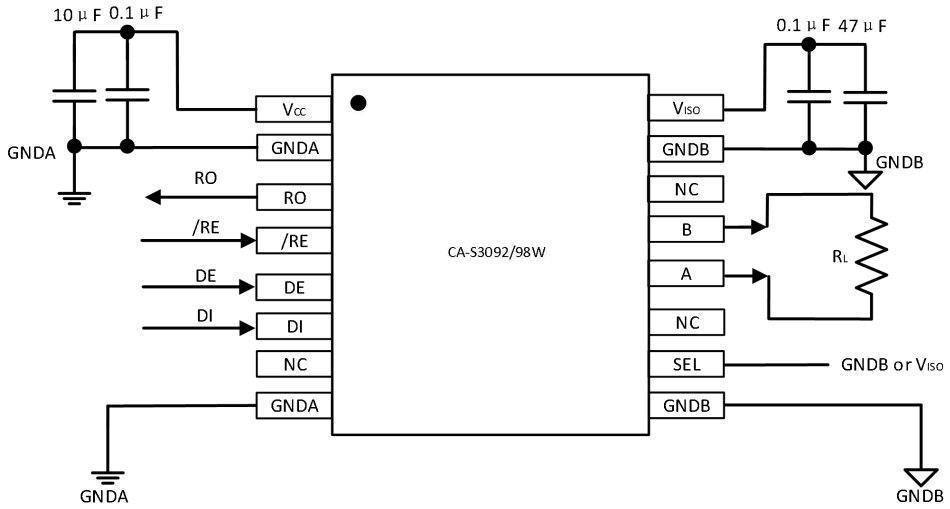
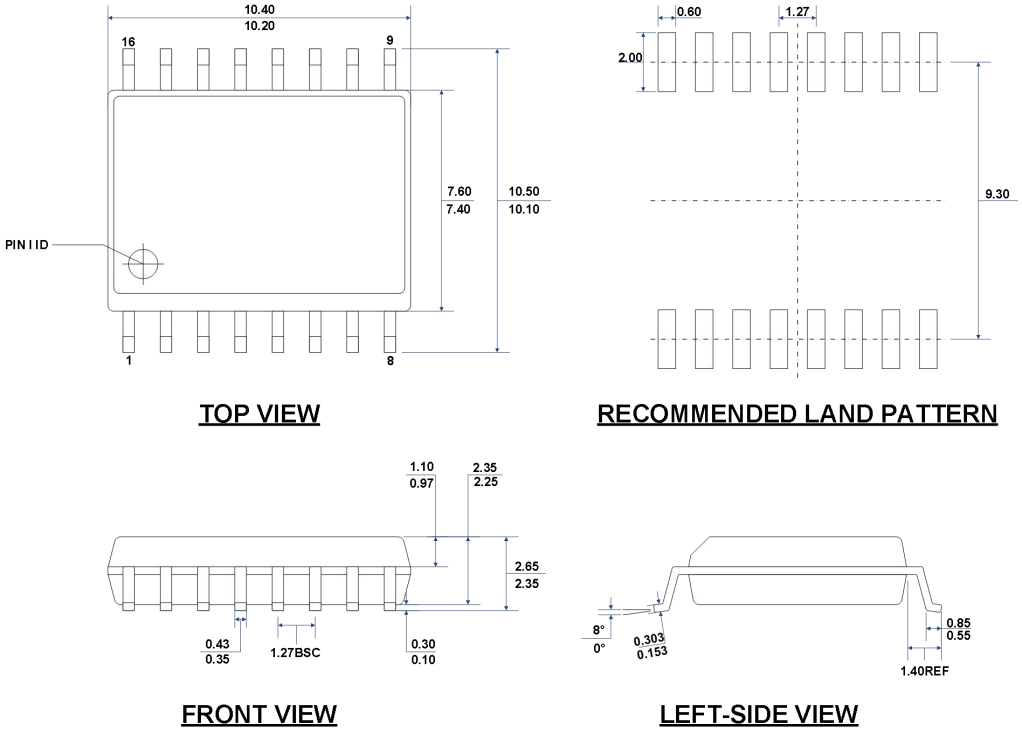


Figure 12- 3 CA-IS3092/98W Typical Application Circuit

13. Package Information

13.1. 16-Pin Wide Body SOIC Package

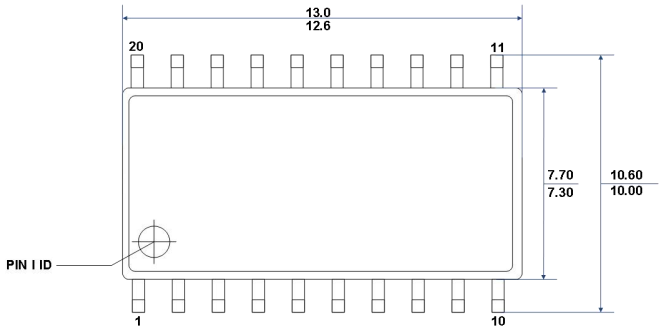
The figure below illustrates the package details and the recommended land pattern details for the CA-IS309xW in a 16-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



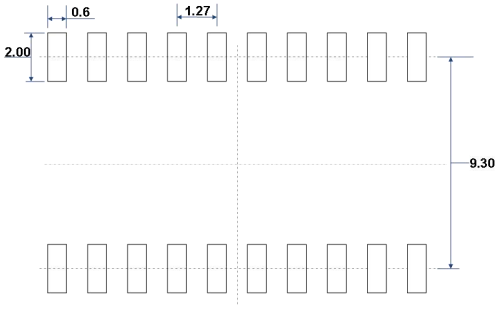
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13.2. 20-Pin Wide Body SOIC Package

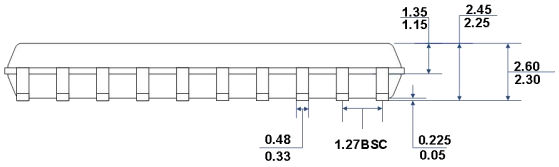
The figure below illustrates the package details and the recommended land pattern details for the CA-IS309xT in a 20-pin wide-body SOIC package. The values for the dimensions are shown in millimeters.



TOP VIEW



RECOMMENDED LAND PATTERN



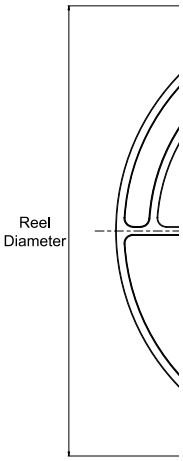
FRONT VIEW



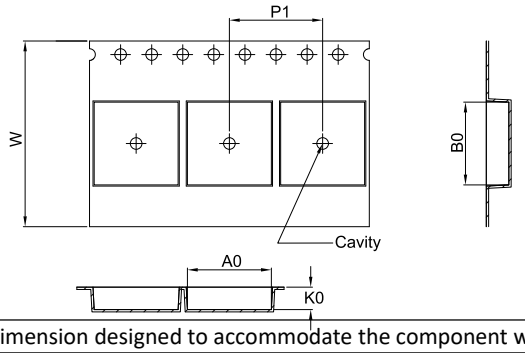
LEFT-SIDE VIEW

14. Tape And Reel Information

REEL DIMENSIONS

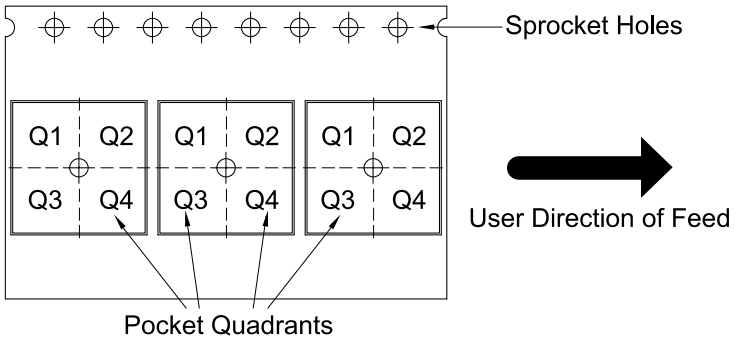


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CA-IS3090W	SOIC	W	16	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3092W	SOIC	W	16	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3096W	SOIC	W	16	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3098W	SOIC	W	16	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3090T	SOIC	W	20	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1
CA-IS3096T	SOIC	W	20	1000	330	24.4	10.8	10.7	2.9	12.0	24.0	Q1

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15. Ordering Information

Orderable Device	Status[1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp(℃)	Device Marking	Samples
CA-IS3090W	PREVIEW	SOIC	W	16	1000				-40 to 125		
CA-IS3092W	PREVIEW	SOIC	W	16	1000				-40 to 125		
CA-IS3096W	PREVIEW	SOIC	W	16	1000				-40 to 125		
CA-IS3098W	PREVIEW	SOIC	W	16	1000				-40 to 125		
CA-IS3090T	PREVIEW	SOIC	W	20	1000				-40 to 125		
CA-IS3096T	PREVIEW	SOIC	W	20	1000				-40 to 125		

1. The marketing status values are defined as follows:
ACTIVE:Product device recommended for new designs.
LIFEBUY:CA has announced that the device will be discontinued,and a lifetime-buy period is in effect.
NRND:Not recommended for new designs.Device is in production to support existing customers,but CA does not recommend using this part in new design.
PREVIEW:Device has been announced but is not in production.Samples may or may not be available.
OBSOLETE:CA has discontinued the production of the device.

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